UART IP Core Specification

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Revision History

4.2 Interrupt Enable Register (IER)

This register allows enabling and disabling interrupt generation by the UART.

Bit #	Access	Description

4.3 Interrupt Identification Register (IIR)

The IIR enables the programmer to retrieve what is the current highest priority pending interrupt.

4.4 FIFO Control Register (FCR)

The FCR allows selection of the FIFO trigger level (the number of bytes in FIFO requiredto enablef theRece

4.5 Line Control Register (LCR)

The line control register allows the specification of the format of the asynchronous data communication used. A bit in the register also allows access to the Divisor Latches,

Bit #	Access	Description

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Operation

This UART core is very similar in operation to the standard 16550 UART chip with the main exception being that only the FIFO mode is supported. The scratch register is removed, as it serves no purpose.

5.1 Initialization

Upon reset the core performs the following tasks:

- The receiver and transmitter FIFOs are cleared.
- The receiver and transmitter shift registers are cleared
- The Divisor Latch register is set to 0.
- The Line Control Register is set to communication of 8 bits of data, no parity, 1 stop bit.
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