L

c

This design is a very simple implementation of FM Receiver for demodulating Frequency

recovered signal.

C

- **fm**
  The core component, the connector between many component in the PLL loops.

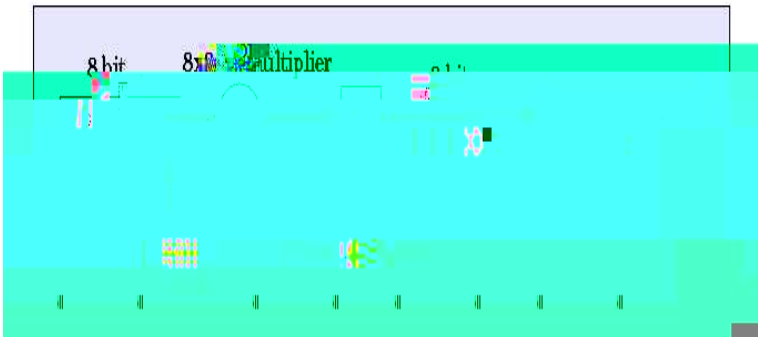

Figure 2-3: Phase detector block diagram

- **loop_ lter**

  A low pass lter in the PLL loop.

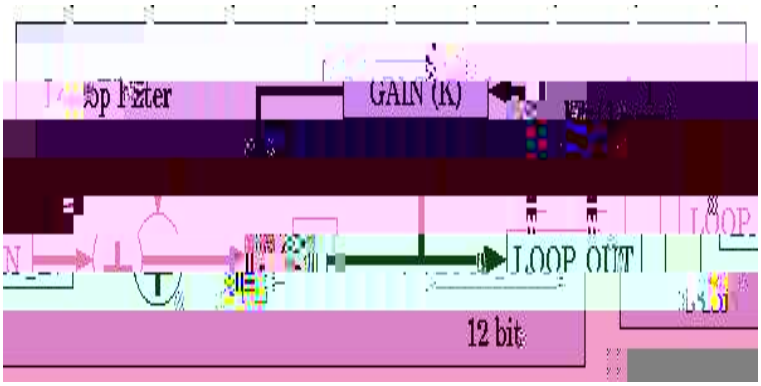

Figure 2-4: Loop lter block diagram

- **adder** **in**

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