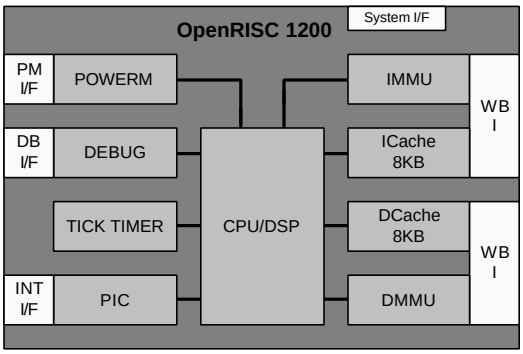
OpenRISC 1200 RISC/DSP Core

Introduction

The OpenRISC 1000 architecture is the latest in the development of modern open architectures and the base for a family of 32- and 64-bit RISC/DSP processors. Open architecture allows a spectrum of chip and system implementations at a variety of price/performance points for a range of applications. Designed with emphasis on performance, simplicity, low power consumption, scalability, and versatility, it targets medium and high performance networking, portable, embedded, and automotive applications.

Features

The OpenRISC 1200 RISC/DSP Core consists of several modular units.



High Performance 32-Bit CPU/DSP

- 32-bit architecture implementing ORBIS32 instruction set
- Scalar, single-issue 5-stage pipeline delivering sustained throughput
- Single-cycle instruction execution on most instructions
- 250 MIPS performance @ 250MHz worst-case conditions
- Predictable execution rate for hard real-time applications
- Fast and deterministic internal interrupt response
- Thirty-two, 32-bit general-purpose registers
- DSP MAC 32x32
- Custom user instructions

L1 Caches

- Harvard model with split instruction and data cache
- Instruction/data cache size scalable from 1KB to 64KB
- Physically tagged and addressed
- Cache management special-purpose registers

Memory Management Unit

- Harvard model with split instruction and data MMU
- Instruction/data TLB size scalable from 16 to 256 entries
- Direct-mapped hash-based TLB
- Linear address space with 32-bit virtual address and physical address from 24 to 32 bits
- Page size 8KB with per-page attributes

Sophisticated Power Management Unit

- Power reduction from 2x to 100x
- Software controlled clock frequency in slow and idle modes
- Interrupt wake-up in doze and sleep modes
- Dynamic clock gating for individual units

Advanced Debug Unit

- Conventional target-debug agent with a debug exception handler
- Non-intrusive debug/trace for both RISC and system

- Real-time trace of RISC and system
- Access and control of debug unit from RISC or via development interface
- Complex chained watchpoint and breakpoint conditions

Integrated Tick Timer

- Task scheduling and precise time measuring
- Maximum timer range of 2^32 clock cycles
- Maskable tick-timer interrupt
- Single-run, restartable or continuous mode

Programmable Interrupt Controller

- 2 non-maskable interrupt sources
- 30 maskable interrupt sources
- two interrupt priorities

Custom and Optional Units

- Additional units such as a floating-point unit can be added as standard units
- 8 custom units can be added and controlled through special-purpose registers or customer instructions

Development Tools Support

- GNU ANSI C, C++, Java and Fortran compilers
- GNU debugger, linker, assembler and utilities
- Architectural simulator

Operating System Support

- Linux
- uClinux
- OAR RTEMS real-time OS

Leading 3rd party products such as Windows CE and VxWorks are planned to be available.

Specifications

- 250 MHz in worst-case 0.18u 6LM

System Interface

- System interface optimized for system-on-chip applications
- Low-latency, open-standard dual WISHBONE interface
- Dual interface – simultaneous flow of instructions and data
- Variety of peripheral cores optimized for transparent interconnection with the OpenRISC 1200

General Description

The OpenRISC 1200 Processor Core is ideally suited for applications that require 32-bit performance compared to performance of 16-bit processors and need low cost and low power consumption advantage compared to 64-bit processors.

- 250 MIPS Dhrystone 2.1 @ 250MHz wc
- 250 MMAC operations @ 250MHz wc
- <1W @ 250MHz, 0.18u, full throttle (est)
- <500mW @ 250MHz, 0.18u, half throttle (est)
- Area <0.5 sqmm @ 0.18u 6LM (cache memories not included)

Target Applications

- Internet, networking and telecom applications
- Embedded applications
- Portable and wireless applications
- Home entertainment consumer electronics
- Automotive applications

Utilization

The table in this section lists the intended applications of the different cores.

Core	FPGA Size	Silicon Area	Speed	Power Consumption