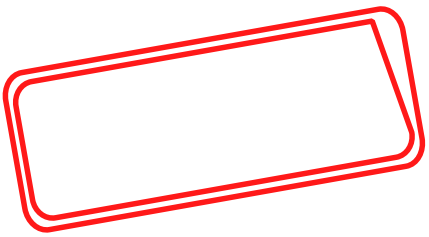

VGA/LCD Core v2.0 Specifications

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1 Introduction

Features

- **CRT and LCD display support**
- **Separate VSYNC/HSYNC and**

rst_i is not a WISHBONE-compatible signal. It is primarily provided for FPGA implementations. Using [rst_i] instead of [wb_rst_i] can result in lower cell usage and

3.3 Control Register [CTRL]

Bit #	Access	Description

3.3.5 CSL

The Composite Sync Polarization Level defines the voltage level of the composite

3.4.6 HINT

The Horizontal Interrupt Pending flag is set (‘1’) when the horizontal synchronization pulse [hsync_pad_o] is asserted. When the HIE bit is set (‘1’) and HINT is asserted, the host system is interrupted. Software must clear the interrupt by writing a (‘0’) to this bit.

3.4.7 LUINT

3.5.3 Thgate

The horizontal gate width, measured in pixels -1.
Example: Thgs -8lae

bit 15	bit 14:8	bit 7:0	
0	Color Data		Color mode
1	always zero	Alpha Data	Alpha / Transparency mode

5
Architecture

up Table7(y)12ture